IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A method for polishing or planarizing a surface of a semiconductor device structure, comprising:

magnetically biasing rigid, independently movable pressurization structures to individually apply a plurality of different amounts of pressure to different, discrete locations of a backside of the semiconductor device structure by magnetically repelling at least one of the rigid, independently movable pressurization structures toward the backside or by magnetically attracting at least one of the rigid, independently movable pressurization structures toward the backside; and

polishing or planarizing at least one layer on the surface of the semiconductor device structure.

2-6. (Canceled)

7. (Currently amended) A method for polishing or planarizing a surface of a semiconductor device structure, comprising:

biasing rigid, independently movable pressurization structures to individually apply a plurality of different amounts of pressure to different, discrete locations of a backside of the semiconductor device structure, comprising ~~The method of claim 1, wherein biasing comprises~~ selectively applying a negative pressure to at least one of the rigid, independently movable pressurization structures; and

polishing or planarizing at least one layer on the surface of the semiconductor device structure.

8. (Canceled)

9. (Previously presented) The method of claim 1, wherein polishing or planarizing comprises chemical-mechanical polishing.

10. (Previously presented) The method of claim 1, wherein biasing and polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure.

11. (Original) The method of claim 1, further comprising locating at least one raised area on an active surface of the semiconductor device structure.

12. (Previously presented) The method of claim 11, wherein biasing includes applying an appropriate amount of pressure to the backside of the semiconductor device structure, opposite the at least one raised area so as to planarize the active surface during the polishing or planarizing.

13. (Previously presented) The method of claim 11, wherein biasing includes individually applying pressure to a backside of another semiconductor device structure of the same type as the semiconductor device structure, opposite a location of the at least one raised area of the semiconductor device structure.

14. (Previously presented) The method of claim 13, wherein polishing or planarizing comprises forming a substantially planar surface on the another semiconductor device structure.

15. (Original) The method of claim 1, comprising substantially simultaneously applying the plurality of different amounts of pressure to the backside of the semiconductor device structure.

16. (Previously presented) A method for polishing at least one layer on a semiconductor device structure, comprising:

polishing at least one layer of a first semiconductor device structure;

locating any raised areas on the first semiconductor device structure following the polishing;

individually applying pressure to a backside of at least one second semiconductor device structure of a same type as the first semiconductor device structure, the individually applying being effected at locations beneath areas of the at least one second semiconductor device structure that correspond to the raised areas of the first semiconductor device structure; and

at least mechanically polishing at least one layer of the at least one second semiconductor device structure.

17. (Previously presented) The method of claim 16, wherein locating comprises employing metrology techniques.

18. (Previously presented) The method of claim 16, wherein individually applying comprises applying a sufficient amount of pressure at each of the locations to form a substantially planar surface on the at least one second semiconductor device structure.

19. (Previously presented) The method of claim 16, wherein individually applying comprises individually applying different amounts of pressure at different ones of the locations.

20. (Previously presented) The method of claim 16, wherein individually applying comprises determining an appropriate amount of pressure to apply to each of the locations based on a height of each corresponding raised area.

21. (Previously presented) The method of claim 16, wherein individually applying comprises selectively applying pressure to the backside of the at least one second semiconductor device structure to at least one annular location.

22. (Previously presented) The method of claim 16, wherein polishing comprises mechanically polishing the at least one layer of the first semiconductor device structure.

23. (Previously presented) The method of claim 16, wherein polishing comprises chemical-mechanical polishing the at least one layer of the first semiconductor device structure.

24. (Previously presented) The method of claim 16, wherein at least mechanically polishing comprises chemical-mechanical polishing the at least one layer of the at least one second semiconductor device structure.

25. (Previously presented) The method of claim 16, wherein individually applying comprises biasing at least one rigid pressurization structure against the backside of the at least one second semiconductor device structure.

26. (Previously presented) The method of claim 25, wherein biasing comprises employing a magnet to bias the at least one pressurization structure against the backside.

27. (Previously presented) The method of claim 26, wherein employing the magnet comprises repelling the at least one pressurization structure toward the backside to effect biasing.

28. (Previously presented) The method of claim 26, wherein employing the magnet comprises attracting the at least one pressurization structure toward the backside to effect biasing.

29. (Previously presented) The method of claim 25, wherein biasing comprises resiliently biasing the at least one pressurization structure against the backside.

30. (Previously presented) The method of claim 29, wherein individually applying further comprises applying a negative pressure to the at least one pressurization structure.

31. (Previously presented) The method of claim 25, wherein biasing comprises applying a selected amount of positive pressure to the at least one pressurization structure.

32. (New) The method of claim 7, wherein polishing or planarizing comprises chemical-mechanical polishing.

33. (New) The method of claim 7, wherein biasing and polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure.

34. (New) The method of claim 7, further comprising locating at least one raised area on an active surface of the semiconductor device structure.

35. (New) The method of claim 34, wherein biasing includes applying an appropriate amount of pressure to the backside of the semiconductor device structure, opposite the at least one raised area so as to planarize the active surface during the polishing or planarizing.